H-A

Notice of Allowability	Application No.	Applicant(s)	
	10/658,707	TSAI ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 10 January 2005*.

2. ☒ The allowed claim(s) is/are *1-14,16-19 and 21-26*.

3. ☒ The drawings filed on *08 September 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

AMIR ZAHARIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

This office action is in response to the filing of the amendment on 10 January 2005. Claims 1-14, 16-19 and 21-26 are pending; claims 15 and 20 have been cancelled.

Allowable Subject Matter

Claims 1-14, 16-19 and 21-26 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a method for forming a dual damascene structure in a semiconductor device manufacturing process where a process wafer comprises a via opening extending through at least one dielectric insulating layer; forming a first photoresist layer on the process wafer surface to include filling the via opening; forming a second photoresist layer over the first photoresist layer; photolithographically patterning the second photoresist layer to form a trench opening etching pattern; forming a via plug comprising the first photoresist layer wherein the first and second photoresist layers respectively comprise different types of photoresist selected from the group consisting of positive and negative photoresists; and, etching a trench opening according to the trench opening etching pattern.

For example, Hung et al. (6,380,096) disclose a method for forming a dual damascene structure semiconductor device where a via opening is formed extending

through at least one dielectric insulating layer; blanket depositing an anti-reflective coating (ARC) layer to include filling the via opening; blanket depositing a photoresist layer over and contacting the ARC layer; photolithographically patterning the photoresist layer form a trench opening etching pattern overlying and encompassing the via opening; etching back the ARC layer to form a via plug having a predetermined thickness partially filling the via opening, wherein the via plug is formed to fill the via opening to a level at about where a bottom portion of the trench opening is formed; and etching a trench opening according to the trench opening etching pattern.

However, Hung et al. do not disclose, anticipate, teach, or suggest forming a first photoresist layer on the process wafer surface to include filling the via opening; and forming a second photoresist layer over the first photoresist layer, wherein the first and second photoresist layers respectively comprise different types of photoresist selected from the group consisting of positive and negative photoresists.

Nam (2004/0121578) discloses a method for forming a dual damascene structure in a semiconductor device manufacturing process where a process wafer comprises a via opening (18) extending through at least one dielectric insulating layer (13, 15); forming a first photoresist layer (16) on the process wafer surface to include filling the via opening (18); forming a second photoresist layer (26); photolithographically patterning the second photoresist layer (26) to form a trench opening etching pattern (27); and etching a trench opening (19) according to the trench opening etching pattern (27) (para. 32-40). However, Nam does not disclose, anticipate, teach or suggest forming a second photoresist layer over the first photoresist layer; and forming a via

plug comprising the first photoresist layer wherein the first and second photoresist layers respectively comprise different types of photoresist selected from the group consisting of positive and negative photoresists.

The prior art made of record in this action does not anticipate, teach, or suggest a method for forming a dual damascene structure in a semiconductor device manufacturing process where a process wafer comprises a via opening extending through at least one dielectric insulating layer; forming a first photoresist layer on the process wafer surface to include filling the via opening; forming a second photoresist layer over the first photoresist layer; photolithographically patterning the second photoresist layer to form a trench opening etching pattern; forming a via plug comprising the first photoresist layer wherein the first and second photoresist layers respectively comprise different types of photoresist selected from the group consisting of positive and negative photoresists; and, etching a trench opening according to the trench opening etching pattern.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571)

272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800